Claims:

1. A high-density circuit module comprising:

a first CSP having upper and lower major surfaces and a first and a second edge, the edges delineating a lateral extent for the upper major surface;

a second CSP;

a form standard disposed between the first and second CSPs, the form standard having a lateral extent greater than the lateral extent of the upper major surface of the first CSPs, the form standard presenting at least one surface for contact with flex circuitry, the flex circuitry connecting the first and second CSPs and disposed to place a first portion of the flex circuitry beneath the lower major surface of the first CSP and a second portion of the flex circuitry above the form standard disposed between the first and second CSPs.

2. The high-density circuit module of claim 1 in which the flex circuitry comprises at least one flex circuit having first and second conductive layers, between which there is an intermediate layer, the second conductive layer having demarked first and second flex contacts, the first flex contacts in electrical connection with the first CSP and the second flex contacts in electrical connection with the second CSP.

3. The high-density circuit module of claim 1 in which the flex circuitry comprises a conductive layer that expresses first and second flex contacts for connection of the first and second CSPs.

4. A high-density circuit module comprising:

flex circuitry having at least one conductive layer, an outer layer, and first and second flex contacts;

a first CSP having CSP contacts, the CSP contacts of the first CSP contacting the flex circuitry;

a form standard presenting at least one surface for contact with the flex circuitry;

a second CSP having CSP contacts, the first CSP being disposed above the form standard and the second CSP and the CSP contacts of the second CSP contacting the flex circuitry.

5. The module of claim 4 in which the form standard presents at least one curved surface for contact with flex circuitry.

6. A high-density circuit module comprising:

a first CSP having an upper and a lower major surface and a set of CSP contacts along the lower major surface;

a second CSP having first and second lateral edges and upper and lower major surfaces and a set of CSP contacts along the lower major surface, the first and second lateral edges delineating an extent of the upper major surface of the second CSP and the first CSP being disposed above the second CSP;

flex circuitry connecting the first and second CSPs; and

a form standard having an extent greater than the extent of the upper major surface of the second CSP and disposed so as to extend between the first and second CSPs and beyond the extent of the upper major surface of the second CSP.

7. A high-density circuit module comprising:

a first CSP having first and second major surfaces with a plurality of CSP contacts along the first major surface;

a second CSP having first and second major surfaces with a plurality of CSP contacts along the first major surface,

a form standard, the first CSP being disposed above the form standard and the second CSP, the form standard presenting an at least one curved surface for contact with a pair of flex circuits, the pair of flex circuits each having first and second conductive layers between which conductive layers there is an intermediate layer, the second conductive layer having demarked a plurality of upper and lower flex contacts a set of said plurality of upper and lower flex contacts being connected to the first conductive layer, and a second set of said plurality of upper and lower flex contacts being comprised of selected ones of upper flex contacts that are connected to corresponding selected ones of lower flex contacts, the plurality of CSP contacts of the first CSP being in contact with the upper flex contacts and the plurality of CSP contacts of the second CSP being in contact with the lower flex contacts.

8. The high density circuit module of claim 7 in which the first and second CSPs are memory circuits.

9. The high-density circuit module of claim 7 in which:

a data set of the plurality of CSP contacts of the first CSP express an n-bit datapath;

a data set of the plurality of CSP contacts of the second CSP express an n-bit datapath:

each of the flex circuits of the pair of flex circuits has supplemental lower flex contacts which, in combination with the lower flex contacts, provide connection for the set of module contacts and a set of supplemental module contacts to express a 2n-bit module datapath that combines the n-bit datapath expressed by the data set of the plurality of CSP contacts of the first CSP and the n-bit datapath expressed by the data set of the plurality of CSP contacts of the second CSP.

10. The high-density circuit module of claim 7 in which the second set of said plurality of upper and lower flex contacts is connected to the first conductive layer with vias that pass through the intermediate layer.

11. The high-density circuit module of claim 10 in which the second set of said plurality of upper and lower flex contacts is comprised of upper flex contacts connected to the first conductive layer with on-pad vias.

12. The high-density circuit module of claim 10 in which the second set of said plurality of upper and lower flex contacts is comprised of lower flex contacts connected to the first conductive layer with off-pad vias.

13. A memory access system comprising:

a memory expansion board;

a high-density circuit module devised in accordance with claim 6, the high-density circuit module being mounted on the memory expansion board;

a switching multiplexer mounted on the memory expansion board, the switching multiplexer for switching data lines between the first and second CSPs; and

a decode logic circuit for decoding chip selection signals from a control circuit and providing a switching multiplexer control signal.

14. A memory access system comprising:

a high-density circuit module having plural CSPs and devised in accordance with claim 6;

a switch for connecting a datapath to one of the plural CSPs of the high-density circuit module;

a decode logic for generating a control signal that causes the switch to connect the datapath to one of the plural CSPs in response to a combination signal comprised of a clock signal and a chip select signal.

15. The memory access system of claim 14 in which the plural CSPs of the high-density circuit module number four.

16. A memory access system comprising:

plural memory expansion boards each populated with plural high-density circuit modules, each of which plural high-density circuit modules being devised with plural CSPs in accordance with claim 6;

plural multiplexers mounted upon each of the plural memory expansion boards, the plural multiplexers for making connections between a datapath and single ones of the plural CSPs comprising the high-density circuit modules;

decode logic on each of the plural memory expansion boards, the decode logic for generating a control signal in response to a combination signal comprised of a clock signal and a chip select signal, the control signal causing at least one of the plural multiplexers to connect a particular datapath to a particular one of the plural CSPs.

17. The memory access system of claim 16 in which the multiplexers are FET multiplexers.

18. The memory access system of claim 16 in which the plural high-density circuit modules are devised in accordance with claim 1.

19. The memory access system of claim 16 in which the plural high-density circuit modules are comprised of four CSPs.

20. The memory access system of claim 16 in which the plural high-density circuit modules are comprised from two CSPs.

21. A memory access system comprising:

a memory board having a board memory signal data connection that provides a connection for memory signals between a plurality of CSPs mounted on the memory board and memory control circuitry;

a high-density circuit module comprised of first, second, third, and fourth individual CSPs, the high-density circuit module being mounted on the memory board and devised in accordance with claim 6;

a switching multiplexer mounted on the memory board, the switching multiplexer having a set of plural input data connections, individual ones of the plural input data connections connected to provide individual data connections between each of the first, second, third, and fourth individual CSPs and the switching multiplexer; and

a decode logic circuit for decoding chip selection signals from a control circuit and providing a switching multiplexer control signal.

22. The memory access system of claim 21 in which the switching multiplexer further comprises an output data connection connected to the board signal memory data connection.

23. The memory access system of claim 22 in which the switching multiplexer provides selective individual connection between the board signal memory data connection and the first, second, third, and fourth individual CSPs.

24. The memory access system of claim 23 in which the individual connection between the board signal memory data connection and the first, second, third, and fourth individual CSPs occurs in response to the switching multiplexer control signal from the decode logic circuit.

25. The memory access system of claim 21 in which the decode logic circuit is mounted on the memory board.

26. The memory access system of claim 21 in which the high-density memory module is devised in accordance with claim 1.

27. A memory access system comprising:

X memory expansion boards each populated with Y high-density circuit modules devised in accordance with claim 6, each of which Y high-density circuit modules being comprised of Z individual CSPs;

plural multiplexers mounted upon each of the X memory expansion boards, the plural multiplexers each for selectively making connections between a datapath

and single ones of the Z CSPs comprising each of the Y high-density circuit modules;

decode logic on each of the plural memory expansion boards, the decode logic for generating a control signal in response to a combination signal comprised of a clock signal and a chip select signal, the control signal causing at least one of the plural multiplexers to connect a particular datapath to a particular one of the Z CSPs.

28. The memory access system of claim 27 in which the multiplexers are FET multiplexers.

29. The memory access system of claim 27 in which the Y high-density circuit modules are devised in accordance with claim 1.

30. The memory access system of claim 27 in which Z equals 4.

31. The memory access system of claim 27 in which Z equals 2.